(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 357 522 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.06.2015 Bulletin 2015/26

(51) Int Cl.:
G02F 1/1362 *(2006.01)* ***G02F 1/13*** *(2006.01)*

(21) Application number: **10170945.9**

(22) Date of filing: **27.07.2010**

(54) **Polymer stabilization alignment liquid crystal display panel and liquid crystal display panel**

Polymerstabilisierungsausrichtungsflüssigkristallanzeigetafel und Flüssigkristallanzeigetrafel

Panneau d'affichage à cristaux liquides à alignement de stabilisation de polymères et panneau d'affichage à cristaux liquides

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

(30) Priority: **22.12.2009 TW 098144291**

(43) Date of publication of application:
17.08.2011 Bulletin 2011/33

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Description

[0001] This application claims the right of priority based on Taiwan Patent Application No. 098144291 entitled "Polymer Stabilization Alignment Liquid Crystal Display Panel and Liquid Crystal Display Panel", filed on Dec. 22, 2009, and assigned to the assignee herein.

BACKGROUND

1. Technical Field

[0002] The present invention relates to a liquid crystal display panel, and more particularly to a pixel structure of a polymer stabilization alignment (PSA) liquid crystal display (LCD) panel.

2. Description of the Related Art

[0003] With the development of flat panel display technique, flat panel displays, such as liquid crystal displays that have advantages of light weight, small size and low power consumption are becoming more and more popular. However, under a circumstance that a pretilt angle of the liquid crystal is not set, when liquid crystal is rotated, the liquid crystal may irregularly rotate left or right to form a disordered arrangement, and thus a contrast ratio of the liquid crystal display is severely reduced. In order to control the arrangement of the liquid crystal, an alignment film is disposed on an inner side of a substrate plate in a process of making the liquid crystal display. Generally, a rubbing method is widely adopted to form the alignment film. In the rubbing method, a polymer resin film, such as polyimide resin film is rubbed by fabrics or the like along a single direction, thereby enabling the polyimide resin molecules to align in desired directions. However, the alignment film made by the rubbing method has some disadvantages, such as being polluted by impurities, reducing output due to static electricity, and reducing contrast ratio due to the contact while rubbing.

[0004] In order to solve above-mentioned problems, various un-rubbing methods that might form an alignment film have emerged, wherein a polymer stabilization alignment method is widely applied for advantages of simple process, low contact pollution, and little light leakage. In the polymer stabilization alignment method, a reactant monomer is mixed into the liquid crystal, and a color filter (CF) substrate and a thin film transistor (TFT) array substrate are positioned on opposite sides of the liquid crystal and fixed together by curing adhesives. Because pixel electrodes of the liquid crystal display have a plurality of slits formed therebetween and aligned in predetermined directions, when a voltage is applied on upside and downside of the liquid crystal, the liquid crystal molecules can be aligned at pretilt angles. In addition, after the reactant monomer is solidified by ultraviolet (UV) curing, a stabilization alignment polymer film having a fixed pretilt angle is formed on an inner side of the CF substrate and/or TFT array substrate.

[0005] However, according to a test result of Multi-domain Vertical Alignment (MVA) liquid crystal display panel, an aperture ratio and a brightness of a traditional MVA liquid crystal display panel still remain to be improved, and how to develop along directions of high contrast ratio, little color shift, high luminance, rapid reaction and wide visual angle of the liquid crystal display is still a big subject.

[0006] U.S. patent application US 2007/076147 A1 discloses a polymer stabilization alignment LCD panel comprising a first substrate plate (insulating transparent glass substrate); a plurality of gate lines (scan lines) disposed on the first substrate plate; a plurality of data lines (signal lines) disposed on the first substrate plate, and substantially perpendicular to the gate lines, the gate lines and the data lines cooperatively defining a plurality of pixel regions, each pixel region comprising at least a main display region (transmissive portion) and a sub display region (reflective portion); a dielectric layer (interlayer film) positioned on the gate lines and the data lines; a plurality of first pixel electrodes positioned in the main display region and on the dielectric layer, each first pixel electrode electrically connecting to the corresponding gate line and data line, and each first pixel electrode being separated from the adjacent data line and thereby forming a gap therebetween; a plurality of second pixel electrodes positioned in the sub display region and on the dielectric layer, each second pixel electrode electrically connecting to the corresponding gate line and data line; a second substrate plate (second insulating transparent glass substrate) positioned opposite to the first substrate plate; and a liquid crystal layer positioned between the first substrate plate and the second substrate plate. With this structure, the pixel electrode located on the transmissive portion side partly overlaps the scan line. Thus, even when a potential difference produced between the scan line and a common electrode makes liquid crystal molecules existing near the scan line inclined all the time, its effects can be efficiently suppressed by the pixel electrode. This makes it possible to obtain a VA (vertically aligned) or MVA semi-transmissive LCD panel that suffers less from crosstalk and that offers bright display with wide viewing angle and high contrast.

[0007] European patent application EP 1 736 818 A1 discloses a semi-transmissive liquid crystal display device comprising a first substrate which is partitioned by signal lines and scanning lines provided in a matrix pattern in which a reflective part and a transmissive part are formed on respective positions, a second substrate which is formed with a color filter and a common electrode, and a liquid crystal layer which is provided in between said two substrates, a pixel electrode which is provided on said reflective part and said transmissive part being formed so as to overlap with said scanning lines and said signal lines via an interlayer film when viewed from the upper side, a width of the signal lines in said transmissive part being broader than a width of the signal lines corre-

sponding to said reflective part, and an overlapping width of the pixel electrode and a signal line in said transmissive part being broader than an overlapping width of the pixel electrode and a signal line in said reflective part. As a result, it will be possible to provide a semi-transmissive LCD device having good contrast without any negative effects on display quality such as cross-talk or the like.

[0008] U.S. patent application US 2008/0179565 A1 and US 2006/0279670 A1 also disclose LCD panels.

BRIEF SUMMARY

[0009] The present invention provides a liquid crystal display panel as defined by the claims and a liquid crystal display panel that may solve one or more of the above-mentioned disadvantages.

[0010] The present invention not only can control the liquid crystal molecules located near the data lines well, but also increase the aperture ratio. Therefore, the display effect of the liquid crystal display panel can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and other features and advantages of the various embodiments disclosed herein will be better understood with respect to the following description and drawings, in which like numbers refer to like parts throughout, and in which:

FIGS. 1A and 1B are top plan schematic views of a liquid crystal display panel according to a first embodiment of the present invention.

FIGS. 2A and 2B are cross-sectional schematic views of the liquid crystal display panel of FIG. 1A, taken along lines I-I' and II- II' respectively.

FIG. 3A is a cross-sectional schematic view of a junction portion of a first pixel and a data line of a liquid crystal display panel, according to a second embodiment of the present invention.

FIG. 3B is a cross-sectional schematic view of a junction portion of a second pixel and a data line of the liquid crystal display panel, according to the second embodiment of the present invention.

FIG. 4A is a cross-sectional schematic view of a junction portion of a first pixel and a data line of a liquid crystal display panel, according to a third embodiment of the present invention.

FIG. 4B is a cross-sectional schematic view of a junction portion of a second pixel and a data line of the liquid crystal display panel, according to the third embodiment of the present invention.

FIG. 5A is a cross-sectional schematic view of a junction portion of a first pixel and a data line of a liquid crystal display panel, according to a fourth embodiment of the present invention.

FIG. 5B is a cross-sectional schematic view of a junction portion of a second pixel and a data line of the liquid crystal display panel, according to the fourth embodiment of the present invention.

FIG. 6 is a distribution schematic view of a junction portion of a second pixel and a data line of a liquid crystal display panel, according to a fifth embodiment of the present invention.

FIG. 7 is a cross-sectional schematic view of the liquid crystal display panel of FIG. 6, taken along line III-III'.

FIG. 8 is a distribution schematic view of a junction portion of a second pixel and a data line of a liquid crystal display panel, according to a comparison example.

FIG. 9 is a cross-sectional schematic view of the liquid crystal display panel of FIG. 8, taken along line IV-IV'.

DETAILED DESCRIPTION

[0012] Reference will now be made to the drawings and various exemplary embodiments to describe the present polymer stabilization alignment liquid crystal display panel and liquid crystal display panel in detail. The embodiments provided in the detailed description should not unduly limit the scope of the claims. The description of every member should not limit the member to a specific practice mode and position. Any practice modes recombined by members and methods producing equality effects, should be covered by the scope of the present invention.

Embodiments:

[0013] FIG.1A is a top plan schematic view of a liquid crystal display panel according to a first embodiment of the present invention, FIGS. 2A and 2B are cross-sectional schematic views of the liquid crystal display panel of FIG. 1A, taken along lines I-I' and II- II' respectively. Referring to FIGS. 1A, 2A and 2B, a liquid crystal display panel 200 of the present invention may be any types of liquid crystal display panels, and preferably is a polymer stabilization alignment (PSA) liquid crystal display panel. FIG. 1A just shows a single pixel structure 100 for description, and actually, the liquid crystal display panel 200 may include a plurality of pixel structures 100 arranged in array. It should be noted that, the pixel structure 100 may be either a sub-pixel or a whole pixel directly. If the pixel structure 100 is a sub-pixel, a pixel may include a plurality of the pixel structures 100. The pixel structures 100 may be, but are not limited to a red sub-pixel, green sub-pixel, a blue sub-pixel, a white sub-pixel and so on.

[0014] As shown in FIGS. 1A, 2A and 2B, the pixel structure 100 includes two gate lines (also can be referred to as scan lines) GL(x) and GL(x+1), two data lines (also can be referred to as signal lines) DL(y) and DL(y+1), two common electrodes COM(x) and COM(x+1), a dielectric layer 22, a color filter CF, a first pixel electrode PX1, a second pixel electrode PX2, transistors Ta, Tc

and Tb, stabilization alignment polymer films 24 and 32, a substrate plate 30, and a liquid crystal layer LC, which are all formed on a base substrate 20. This embodiment takes, but not limited to the display panel with a color filter incorporated in transistors array substrate (COA) for example to describe the present invention.

[0015] As shown in FIG.1A, the data lines DL(y) and DL(y+1) are substantially perpendicular to the gate lines GL(x) and GL(x+1), but the present invention is not limited as such. The gate lines GL(x) and GL(x+1) and the data lines DL(y) and DL(y+1) may define a plurality of pixel regions, and each pixel region includes at least a main display region A1 and a sub display region A2. The first pixel electrode PX1 and the second pixel electrode PX2 are respectively disposed in the main display region A1 and the sub display region A2. Generally, an operating voltage of the main display region A1 is larger than that of the sub display region A2. In other words, the maximal operating voltage applied on the first pixel electrode PX1 is larger than that applied on the second pixel electrode PX2.

[0016] The transistors Ta and Tc may be switch transistors. Gates of the transistors Ta and Tc may be electrically connected to the gate line GL(x). Sources of the transistors Ta and Tc may be electrically connected to the data line DL(y). A drain of the transistor Ta may be electrically connected to the first pixel electrode PX1, and a drain of the transistor Tc may be electrically connected to the second pixel electrode PX2. A gate of the transistor Tb may be electrically connected to the gate line GL(x+1). A source of the transistor Tb may be electrically connected to the drain of the transistor Tc directly. In other words, the source of the transistor Tb and the drain of the transistor Tc use a common metal block. A drain of the transistor Tb is electrically coupled with the first pixel electrode PX1. The common electrodes COM(x) and COM(x+1) are substantially perpendicular to the data lines DL(y) and DL(y+1), and may include a plurality of branches. The common electrodes COM(x) and COM(x+1) may be respectively coupled with the first pixel electrode PX1 and the second pixel electrode PX2 to form capacitances.

[0017] As shown in FIGS. 2A and 2B, the dielectric layer 22 and the color filter CF may be positioned on the data lines DL(y) and DL(y+1) and the gate lines GL(x) and GL(x+1). The first pixel electrode PX1 and the second pixel electrode PX2 may be positioned on the dielectric layer 22 and the color filter CF. The dielectric layer 22 of this embodiment includes transparent organic materials, and the color filter CF may be used as a dielectric layer by itself. The substrate plate 30 is positioned opposite to the base substrate 20, and the liquid crystal layer LC is positioned between the base substrate 20 and the substrate plate 30. The stabilization alignment polymer film 24 may cover the first pixel electrode PX1 and the second pixel electrode PX2. The stabilization alignment polymer film 32 may cover the substrate plate 30 and a black matrix BM. In other words, the stabilization alignment polymer film 24 is positioned between the base substrate 20 and the liquid crystal layer LC, and the stabilization alignment polymer film 32 is positioned between the substrate plate 30 and the liquid crystal layer LC.

[0018] In a process of fabrication of the stabilization alignment polymer films 24 and 32, a reactant monomer is first mixed into the liquid crystal material, and a color filter (CF) substrate and a thin film transistor (TFT) array substrate are then positioned on opposite sides of the liquid crystal and fixed together by curing adhesives. Because the first pixel electrode PX1 and the second pixel electrode PX2 both have a plurality of slits 14 aligned in predetermined directions, when a voltage, such as an alternating current (AC) voltage, is applied on upside and downside electrodes of the liquid crystal layer LC, the liquid crystal molecules and the reactant monomer can be aligned at pretilt angles. Moreover, after the reactant monomer is solidified by ultraviolet curing, the stabilization alignment polymer films 24 and 32 having fixed pretilt angles are formed on inner sides of the CF substrate and/or TFT array substrate. FIGS. 2A and 2B are just schematic views, the actual directions and degrees of the pretilt angles of the stabilization alignment polymer films 24 and 32 may be varied according to a design requirement of every embodiment.

[0019] Referring to FIG.1A again, the first pixel electrode PX1 has a larger operating voltage and is easily to affect an electric field around the first pixel electrode PX1. Therefore, the first pixel electrode PX1 of the present embodiment can be separated from the adjacent data lines DL(y) and DL(y+1) and thereby forming a gap W1 therebetween. In addition, a black matrix BM can be disposed between the first pixel electrode PX1 and the adjacent first pixel electrode PX1 to shield clearances of the pixel structure 100, and thus avoiding the phenomenon of edge light leakages. On the other hand, the second pixel electrode PX2 of the present embodiment may partially overlap the adjacent data lines DL(y) and DL(y+1) and thereby forming an overlap width 01. In addition, the second pixel electrode PX2 and the adjacent second pixel electrode PX2 may not dispose a black matrix BM therebetween, thus aperture ratios of pixels can be increased.

[0020] According to experiment of an embodiment of the present invention, in order to increase the aperture ratio and effectively control the directions of the liquid crystal molecules, the gap W1 between each first pixel electrode PX1 and the adjacent data lines DL(y) and DL(y+1) can be in a range from 1 micron to 6 microns. For example, the gap W1 shown in FIG. 2A is, but not limited to 3 microns. Alternatively, a ratio of the above gap W1 to the width of each data line DL(y) or DL(y+1) can be in a range from 0.01 to 1. On the other hand, each data line DL(y) or DL(y+1) adjacent to the second pixel electrode PX2 are wider, and the overlap width 01 of each data line DL(y) or DL(y+1) and one of the adjacent second pixel electrodes PX2 can be in a range from 1.5

microns to 8 microns. For example, two second pixel electrodes PX2 shown in FIG. 2B are respectively extended about 4 microns inwards from opposite sides of the adjacent data line DL(y+1), thus covering about 8 microns width of the data line DL(y+1). Alternatively, a ratio of overlap width 01 to the width of each data line DL(y) or DL(y+1) can be in a range from 0.01 to 1.

[0021] The first pixel electrode PX1 and the second pixel electrode PX2 both include a plurality of branches 12, and every two adjacent branches 12 define a slit 14 therebetween, without pixel electrode materials. The first pixel electrode PX1 has a plurality of branches 12a. Each branch 12a of the first pixel electrode PX1 has an edge 122a. The second pixel electrode PX2 has a plurality of branches 12b. Each branch 12b of the second pixel electrode PX2 has an edge 122b. This pixel electrode structure is favorable to solve a problem of color cast of different visual angles. It should be noted that, according to an experiment of the present invention, at least one edge 122b of the branches 12b of the second pixel electrode PX2, preferably one or more edges 122b overlapping the adjacent data lines DL(y) or DL(y+1), can be substantially parallel to the data lines DL(y) and DL(y+1), thereby providing a better control effect of the liquid crystal molecules. In this embodiment, the edges122a of the branches 12a of the first pixel electrode PX1 may not be parallel to the data lines DL(y) and DL(y+1), but inclined at an angle about 45 degrees. In other embodiments, the shapes of the first pixel electrode PX1 and the second pixel electrode PX2 may be changed according to requirements, for example, the edges 122a of the branches 12a of the first pixel electrode PX1 may be parallel to the data lines DL(y) and DL(y+1). The corners 124a, 124b of the branches 12a, 12b of the first pixel electrode PX1 and the second pixel electrode PX2 may be substantially round, but not form a sharp angle with a right angle, an acute angle or an obtuse angle, as shown in Fig. 1B.

[0022] The configuration of the pixel structure 100 is not limited to FIGS. 1A to 2B, in other embodiments, the present invention may be applied on a display panel with a black matrix incorporated in the transistor array substrate (BOA). Two adjacent pixel structures may dispose at least two data lines therebetween, for example, the pixel structure of the liquid crystal display panel may be configured as a structure of two data lines collocated with a gate line (2D1 G). Referring to FIGS. 3A to 5B, FIGS. 3A, 4A and 5A are cross-sectional schematic views of junction portions of first pixels and data lines of liquid crystal display panels, respectively according to a second, a third and a fourth embodiments of the present invention. FIGS. 3B, 4B and 5B are cross-sectional schematic views of junction portions of second pixels and data lines of liquid crystal display panels, respectively according to the second, the third and the fourth embodiments of the present invention.

[0023] As shown in FIGS. 3A and 3B, the difference between the second embodiment and the first embodiment is that a liquid crystal display panel 300 of the second embodiment is a BOA type display panel. A color filter CF and a black matrix BM of the liquid crystal display panel 300 are both directly formed on an inner side of a base substrate 20. In other words, the color filter CF, the black matrix BM, a first pixel electrode PX1, a data line DL(y+1), a gate lines GL(X) and GL(x+1) (not shown in FIGS. 3A and 3B), and transistors Ta, Tc and Tb (not shown in FIGS. 3A and 3B) are all disposed on the same base substrate 20.

[0024] As shown in FIGS. 4A and 4B, the difference between the third embodiment and the first embodiment is that a liquid crystal display panel 400 of the third embodiment may include at least two data lines DL(y+1) and DL(y+2) disposed between adjacent pixel structures. As such, two transistors Ta and Tc in the same pixel structure, which are used for respectively control a main display region A1 and a sub display region A2, may be electrically connected to different data lines DL(y) and DL(y+1). In this embodiment, the first pixel electrode PX1 may be separated from the adjacent data lines DL(y+1) and DL(y+2) and thereby forming a gap W1 therebetween, the gap W1 may be, but not limited to 3 microns as shown in FIG. 4A. The second pixel electrode PX2 may partially overlap the adjacent data lines DL(y+1) and DL(y+2) and thereby forming an overlap width 01. For example, two second pixel electrodes PX2 shown in FIG. 4B are respectively extended about 9 microns inwards from edges of adjacent data lines DL(y+1) and DL(y+2), thus completely covering the data line DL(y+1) with about 8 microns wide and the data line DL(y+2) with about 8 microns wide.

[0025] As shown in FIGS. 5A and 5B, the difference between the fourth embodiment and the third embodiment is that a liquid crystal display panel 500 of the fourth embodiment is a BOA-type display panel. A color filter CF and a black matrix BM of the liquid crystal display panel 500 are both directly formed on an inner side of a base substrate 20.

[0026] A comparison between one embodiment of the present invention and a comparison example will be made below, as an example, to describe advantages of the present invention. Referring to FIGS. 6 to 9, FIG.6 is a distribution schematic view of a junction portion of a second pixel and a data line of a liquid crystal display panel according to a fifth embodiment of the present invention. FIG.7 is a cross-sectional schematic view of the liquid crystal display panel of FIG. 6, taken along line III-III'. FIG. 8 is a distribution schematic view of a junction portion of a second pixel and a data line of a liquid crystal display panel according to a comparison example. FIG. 9 is a cross-sectional schematic view of the liquid crystal display panel of FIG. 8, taken along line IV-IV'.

[0027] As shown in FIGS. 6 and 7, a liquid crystal display panel 600 of the fifth embodiment may include at least two data lines DL(y+1) and DL(y+2) disposed between adjacent pixel structures. A dielectric layer 26 may be positioned between the data lines DL(y+1) and DL(y+2) and a second pixel electrode PX2, and the die-

lectric layer 26 may include a color filter CF, a black matrix BM, a transparent organic material or combinations thereof. A substrate plate 38 may include the above substrate plate 30, a common electrode COM, a stabilization alignment polymer film 32 and a selective black matrix BM (not shown). For example, the liquid crystal display panel 600 may have a structure similar to that shown in FIG. 4B or 5B. In order to more clearly display the arrangement of liquid crystal molecules of a liquid crystal layer LC, FIG. 7 does not show the stabilization alignment polymer films, but actually, the liquid crystal display panel 600 may include above stabilization alignment polymer films 24 and 32 to achieve a better display effect.

[0028] According to the distribution of power lines 40 of the liquid crystal display panel 600 during operating, because the second pixel electrode PX2 of the present embodiment partially overlaps the adjacent data lines DL(y+1) and DL(y+2), the stabilization alignment polymer films disposed on the second pixel electrode PX2 can well control the liquid crystal molecules. Thus, the arrangement of liquid crystal molecules 42 located near the data lines DL(y+1) and DL(y+2) is not easily interfered by an electric field generated by the data lines DL(y+1) and DL(y+2). Therefore, the liquid crystal molecules 42 located near the data lines DL(y+1) and DL(y+2) also can be well controlled. That is, the liquid crystal molecules 42 may be aligned substantially perpendicular to the base substrate 20 and the substrate plate 38, and are not prone to undesired inclines, thus avoiding light leakages. Accordingly, the sub display region A2 of the present invention is not required to dispose black matrixes BM around to shield light, thereby efficiently increasing the aperture ratio.

Comparison example:

[0029] As shown in FIGS. 8 and 9, the difference between the comparison example and embodiments of the present invention is that a second pixel electrode PX2 of a liquid crystal display panel 700 of the comparison example dose not overlap adjacent data lines DL(y+1) and DL(y+2). According to the distribution of power lines 40 of the liquid crystal display panel 700 during operating, an electric field generated by the data lines DL(y+1) and DL(y+2) of the comparison example easily interfere the arrangement of liquid crystal molecules 44 located near the data lines DL(y+1) and DL(y+2). Therefore, the liquid crystal molecules 44 located near the data lines DL(y+1) and DL(y+2) are prone to undesired inclines, thus leading to light leakages. To avoid this condition of light leakages, a black matrix BM should be disposed on the data lines DL(y+1) and DL(y+2) located around a sub display region of the comparison example, and the width of the black matrix BM should be larger at least 3 microns than total width of the data lines DL(y+1) and DL(y+2). Consequently, the aperture ratio may be decreased.

[0030] In summary, each first pixel electrode of various embodiments of the present invention is separated from the adjacent data lines, and each second pixel electrode partially overlaps the adjacent data lines. In the process of fabrication of the stabilization alignment polymer films, the arrangement of the liquid crystal molecules and the reactant monomer is controlled by using shapes of the pixel electrodes, therefore, the arrangement of liquid crystal molecules of a PSA liquid crystal display panel is nearly related to the shapes of the pixel electrodes. The present invention not only can well control the liquid crystal molecules located near the data lines, but also increase the aperture ratio. Therefore, the display effect of the liquid crystal display panel can be improved.

[0031] The above description is given by way of example, and not limitation. Given the above disclosure, one skilled in the art could devise variations that are within the scope of the invention disclosed herein, including configurations ways of the recessed portions and materials and/or designs of the attaching structures. Further, the various features of the embodiments disclosed herein can be used alone, or in varying combinations with each other and are not intended to be limited to the specific combination described herein. Thus, the scope of the claims is not to be limited by the illustrated embodiments.

[0032] The present invention provides a polymer stabilization alignment liquid crystal display panel having a plurality of pixel regions. Each pixel region includes a main region and a sub region, and a first pixel electrode and a second pixel electrode correspond to the main region and the sub region respectively. Each first pixel electrode is separated from the adjacent data line and thereby forming a gap therebetween. Each second pixel electrode partially overlaps the adjacent data line. In addition, each second pixel electrode includes a plurality of branches, and at least one edge of the branches may be parallel to the data lines. Accordingly, the present invention not only can increase the aperture ratio, but also well control the liquid crystal molecules located near the data lines. Therefore, the display quality of the liquid crystal display panel can be improved.

Claims

1. A liquid crystal display panel (200, 300, 400, 500, 600, 700) comprising:

   a first substrate plate (20);
   a plurality of gate lines (GL(x), GL(x+1)) disposed on the first substrate plate (20);
   a plurality of data lines (DL(y), DL(y+1)) disposed on the first substrate plate (20), and substantially perpendicular to the gate lines (GL(x), GL(x+1)), the gate lines (GL(x), GL(x+1)) and the data lines (DL(y), DL(y+1)) cooperatively defining a plurality of pixel regions, each pixel region comprising at least a main display region (A1) and a sub display region (A2);
   a dielectric layer (22, 26) positioned on the gate

lines (GL(x), GL(x+1)) and the data lines (DL(y), DL(y+1));
a plurality of first pixel electrodes (PX1) positioned in the main display region (A1) and on the dielectric layer (22, 26), each first pixel electrode (PX1) electrically connecting to the corresponding gate line (GL(x), GL(x+1)) and data line (DL(y), DL(y+1)), and each first pixel electrode (PX1) being separated from the adjacent data line (DL(y), DL(y+1)) and thereby forming a gap (W1) therebetween;
a plurality of second pixel electrodes (PX2) positioned in the sub display region (A2) and on the dielectric layer(22, 26), each second pixel electrode (PX2) electrically connecting to the corresponding gate line (GL(x), GL(x+1)) and data line (DL(y), DL(y+1));
a second substrate plate (30, 38) positioned opposite to the first substrate plate (20); and
a liquid crystal layer (22, LC) positioned between the first substrate plate (20) and the second substrate plate (30, 38);
characterized by
each second pixel electrode (PX2) partially overlapping the adjacent data line (DL(y), DL(y+1)) and thereby forming an overlap width (O1), wherein an operating voltage of the main display region (A1) is larger than that of the sub display region (A2).

2. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 1, wherein the gap (W1) between each first pixel electrode (PX1) and the adjacent data line (DL(y), DL(y+1)) is in a range from 1 micron to 6 microns.

3. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 1, wherein a ratio of the gap (W1) to the width of each data line (DL(y), DL(y+1)) is in a range from 0.01 to 1.

4. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 1, wherein the overlap width (O1) of each data line (DL(y), DL(y+1)) and one of the adjacent second pixel electrodes (PX2) is in a range from 1.5 microns to 8 microns.

5. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 1, wherein a ratio of the overlap width (O1) to the width of each data line (DL(y), DL(y+1)) is in a range from 0.01 to 1.

6. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 1, wherein the second pixel electrode (PX2) comprises a plurality of branches (12, 12b).

7. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 6, wherein each of the branches (12, 12b) has an edge (122b), and at least one edge (122b) of the branches (12, 12b) is substantially parallel to the data lines (DL(y), DL(y+1)).

8. The liquid crystal display panel (200, 300, 400, 500, 600, 700) as claimed in claim 6, wherein each of the branches (12, 12b) has a corner (124b) being substantially round.

9. The liquid crystal display panel as claimed in claim 1, further comprises a stabilization alignment polymer film (24, 32) covering the first pixel electrodes (PX1) and the second pixel electrodes (PX2).

10. The liquid crystal display panel as claimed in one of claims 1 to 9, further comprises a black matrix (BM) covered by the stabilization alignment polymer film (32), disposed between the first pixel electrode (PX1) and the adjacent first pixel electrode (PX1), incorporated in a transistor array substrate (BOA), and/or directly formed on an inner side of the first substrate plate (20).

Patentansprüche

1. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700), umfassend:

eine erste Substratplatte (20);
eine Mehrzahl von Gate-Leitungen ($GL_{(x)}$, $GL_{(x+1)}$), die auf der ersten Substratplatte (20) angeordnet sind;
eine Mehrzahl von Datenleitungen ($DL_{(y)}$, $DL_{(y+1)}$), die auf der ersten Substratplatte (20) angeordnet sind und im Wesentlichen senkrecht zu den Gate-Leitungen ($GL_{(x)}$, $GL_{(x+1)}$) sind, wobei die Gate-Leitungen ($GL_{(x)}$, $GL_{(x+1)}$) und die Datenleitungen ($DL_{(y)}$, $DL_{(y+1)}$) zusammenwirkend eine Mehrzahl von Pixelbereichen definieren, wobei jeder Pixelbereich wenigstens einen Hauptanzeigebereich (A1) und einen Unteranzeigebereich (A2) umfasst;
eine dielektrische Schicht (22, 26), die auf den Gate-Leitungen ($GL_{(x)}$, $GL_{(x+1)}$) und den Datenleitungen ($DL_{(y)}$, $DL_{(y+1)}$) angeordnet ist;
eine Mehrzahl von ersten Pixelelektroden (PX1), die im Hauptanzeigebereich (A1) und auf der dielektrischen Schicht (22, 26) angeordnet sind, wobei jede erste Pixelelektrode (PX1) elektrisch mit der entsprechenden Gate-Leitung ($GL_{(x)}$, $GL_{(x+1)}$) und der Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) verbunden ist, und wobei jede erste Pixelelektrode (PX1) von der benachbarten Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) getrennt ist und dadurch ein Zwischenraum (W1) dazwischen ausgebildet ist;

eine Mehrzahl von zweiten Pixelelektroden (PX2), die im Unteranzeigebereich (A2) und auf der dielektrischen Schicht (22, 26) angeordnet sind, wobei jede zweite Pixelelektrode (PX2) elektrisch mit der entsprechenden Gate-Leitung ($GL_{(x)}$, $GL_{(x+1)}$) und der Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) verbunden ist;
eine zweite Substratplatte (30, 38), die gegenüberliegend der ersten Substratplatte (20) angeordnet ist; und
eine Flüssigkristallschicht (22, LC), die zwischen der ersten Substratplatte (20) und der zweiten Substratplatte (30, 38) angeordnet ist;
dadurch gekennzeichnet, dass jede zweite Pixelelektrode (PX2) die benachbarte Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) teilweise überlappt und dadurch eine Überlappungsbreite (O1) ausbildet, wobei eine Betriebsspannung des Hauptanzeigebereichs (A1) größer als die des Unteranzeigebereichs (A2) ist.

2. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, wobei der Zwischenraum (W1) zwischen jeder ersten Pixelelektrode (P1) und der benachbarten Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) in einem Bereich von 1 Mikrometer bis 6 Mikrometer liegt.

3. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, wobei ein Verhältnis des Zwischenraums (W1) zur Breite jeder Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) in einem Bereich von 0,01 bis 1 liegt.

4. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, wobei die Überlappungsbreite (O1) jeder Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) und einer der benachbarten zweiten Pixelelektroden (PX2) in einem Bereich von 1,5 Mikrometer bis 8 Mikrometer liegt.

5. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, wobei ein Verhältnis der Überlappungsbreite (O1) zur Breite jeder Datenleitung ($DL_{(y)}$, $DL_{(y+1)}$) in einem Bereich von 0,01 bis 1 liegt.

6. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, wobei die zweite Pixelelektrode (PX2) eine Mehrzahl von Verzweigungen (12, 12b) umfasst.

7. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 6, wobei jede der Verzweigungen (12, 12b) eine Kante (122b) aufweist und wenigstens eine Kante (122b) der Verzweigungen (12, 12b) im Wesentlichen parallel zu den Datenleitungen ($DL_{(y)}$, $DL_{(y+1)}$) ist.

8. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 6, wobei jede der Verzweigungen (12, 12b) eine Ecke (124b) aufweist, die im Wesentlichen rund ist.

9. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach Anspruch 1, ferner umfassend einen Stabilisierungsausrichtungs-Polymerfilm(24, 32), der die ersten Pixelelektroden (PX1) und die zweiten Pixelelektroden (PX2) bedeckt.

10. Flüssigkristallanzeigefeld (200, 300, 400, 500, 600, 700) nach einem der Ansprüche 1 bis 9, ferner umfassend eine Schwarzmatrix (BM), die, vom Stabilisierungsausrichtungs-Polymerfilm (32) bedeckt, zwischen der ersten Pixelelektrode (PX1) und der benachbarten ersten Pixelelektrode (PX1) angeordnet, in einem Transistor-Array-Substrat (BOA) integriert und/oder an einer Innenseite der ersten Substratplatte (20) direkt ausgebildet ist.

Revendications

1. Un panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) comprenant:

une première plaque support (20);
plusieurs lignes de grille ($GL_{(x)}$, $GL_{(x+1)}$) placées sur la première plaque support (20);
plusieurs lignes de données ($DL_{(y)}$, $DL_{(y+1)}$) placées sur la première plaque support (20), et en grande partie perpendiculaire aux lignes de grille ($GL_{(x)}$, $GL_{(x+1)}$), les lignes de grille ($GL_{(x)}$, $GL_{(x+1)}$) et les lignes de données ($DL_{(y)}$, $DL_{(y+1)}$) définissant ensemble plusieurs régions de pixels; chaque région de pixels comprenant au moins une région principale d'affichage (A1) et une sous-région d'affichage (A2);
une couche diélectrique (22, 26) positionnée sur les lignes de grille ($GL_{(x)}$, $GL_{(x+1)}$) et les lignes de données ($DL_{(y)}$, $DL_{(y+1)}$);
plusieurs premières électrodes de pixel (PX1) positionnées dans la région principale d'affichage (A1) et sur la couche diélectrique (22, 26), chaque première électrode de pixel (PX1) étant connectée électriquement à la ligne de grille correspondante ($GL_{(x)}$, $GL_{(x+1)}$) et à la ligne de données correspondante ($DL_{(y)}$, $DL_{(y+1)}$), et chaque première électrode de pixel (PX1) étant séparée de la ligne de données adjacente ($DL_{(y)}$, $DL_{(y+1)}$) et formant ainsi un espace (W1) entre les deux;
plusieurs secondes électrodes de pixel (PX2) positionnées dans la sous-région d'affichage (A2) et sur la couche diélectrique (22, 26), chaque seconde électrode de pixel (PX2) étant connectée électriquement à la ligne de grille correspondante ($GL_{(x)}$, $GL_{(x+1)}$) et à la ligne de don-

nées correspondante ($DL_{(y)}$, $DL_{(y+1)}$);
une seconde plaque support (30, 38) positionnée en face de la première plaque de support (20); et
une couche de cristaux liquides (22, LC) positionnée entre la première plaque support (20) et la seconde plaque support (30, 38);
caractérisé en cela que chaque seconde électrode de pixel (PX2) chevauche partiellement la ligne de données adjacente ($DL_{(y)}$, $DL_{(y+1)}$) et formant ainsi une largeur de chevauchement (O1), une tension de service de la région d'affichage principale (A1) étant plus grande que celle de la sous-région d'affichage (A2).

2. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 dans lequel l'espace (W1) entre chaque première électrode de pixel (PX1) et la ligne de données adjacente ($DL_{(y)}$, $DL_{(y+1)}$) correspond à une plage de 1 micron à 6 microns.

3. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 dans lequel le rapport de l'espace (W1) par rapport à la largeur de chaque ligne de données ($DL_{(y)}$, $DL_{(y+1)}$) correspond à une plage de 0,01 à 1.

4. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 dans lequel la largeur de chevauchement (O1) de chaque ligne de données $DL_{(y)}$, $DL_{(y+1)}$) et de l'une des secondes électrodes de pixel adjacentes (PX2) correspond à une plage de 1,5 microns à 8 microns.

5. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 dans lequel le rapport de la largeur de chevauchement (O1) par rapport à la largeur de chaque ligne de données ($DL_{(y)}$, $DL_{(y+1)}$) correspond à une plage de 0,01 à 1.

6. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 dans lequel la seconde électrode de pixels (PX2) comprend plusieurs branches (12, 12b).

7. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 6 dans lequel chacune des branches (12, 12b) possède un bord (122b) et au moins un bord (122b) des branches (12, 12b) est principalement parallèle aux lignes de données ($DL_{(y)}$, $DL_{(y+1)}$).

8. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 6 dans lequel chacune des branches (12, 12b) possède un coin (124b) principalement rond.

9. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon la revendication 1 comprenant également un film à alignement de stabilisation de polymères (24, 32) couvrant les premières électrodes de pixel (PX1) et les secondes électrodes de pixel (PX2).

10. Panneau d'affichage à cristaux liquides (200, 300, 400, 500, 600, 700) selon l'une des revendications 1 à 9 comprenant également une matrice noire (BM) couverte par le film à alignement de stabilisation de polymères (32), placé entre la première électrode de pixel (PX1) et la première électrode de pixel adjacente (PX1), incorporée dans un support de réseau de transistors (BOA) et/ou directement formée sur un côté intérieur de la première plaque support (20).

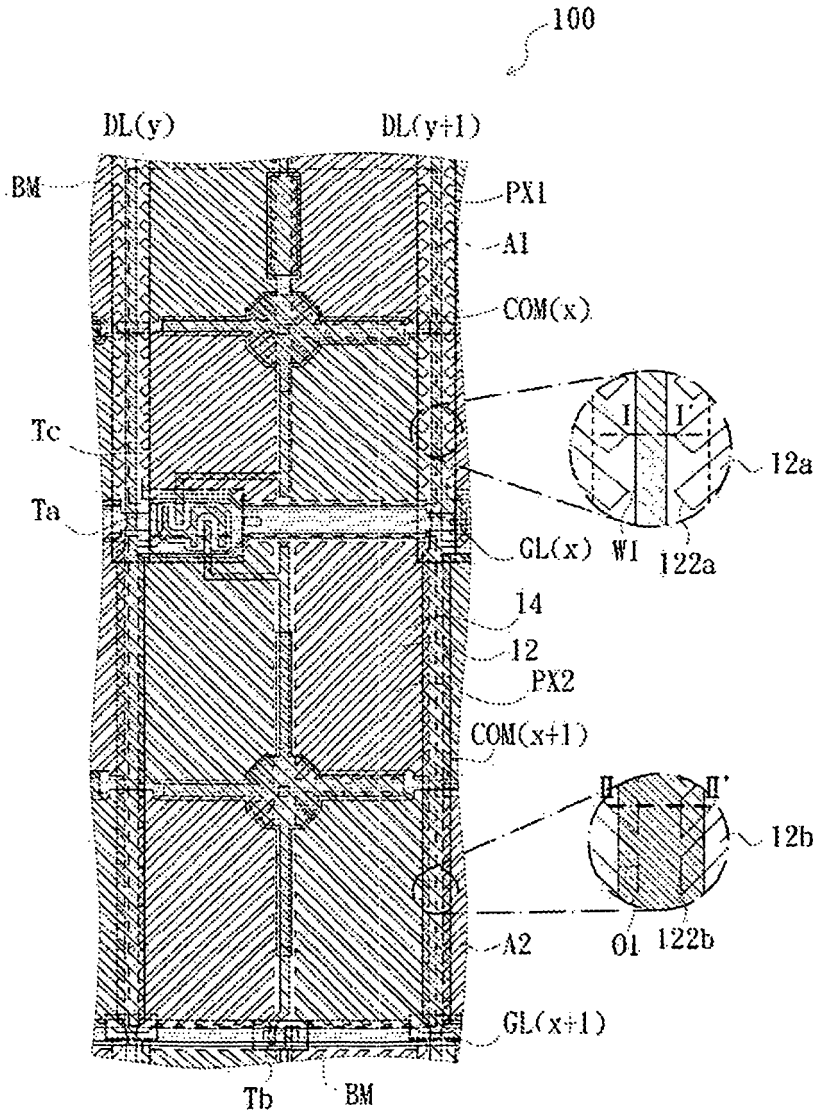
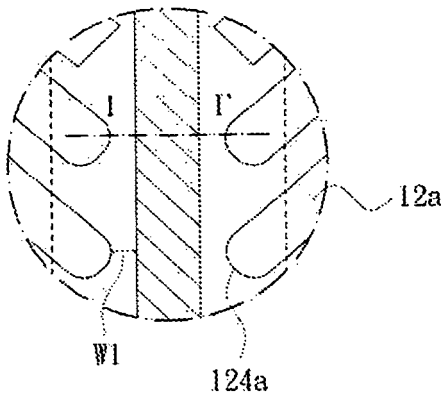

100
DL(y)
DL(y+1)
BM
PX1
A1
COM(x)
Tc
Ta
I
I'
12a
GL(x)
W1
122a
14
12
PX2
COM(x+1)
II
II'
12b
A2
O1
122b
GL(x+1)
Tb
BM

FIG. 1A



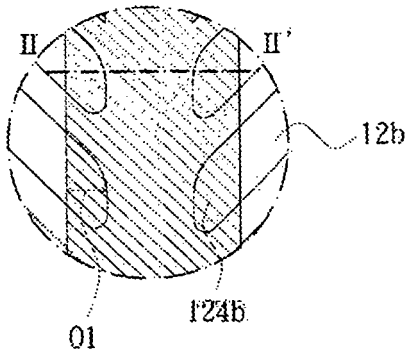


FIG. 1B

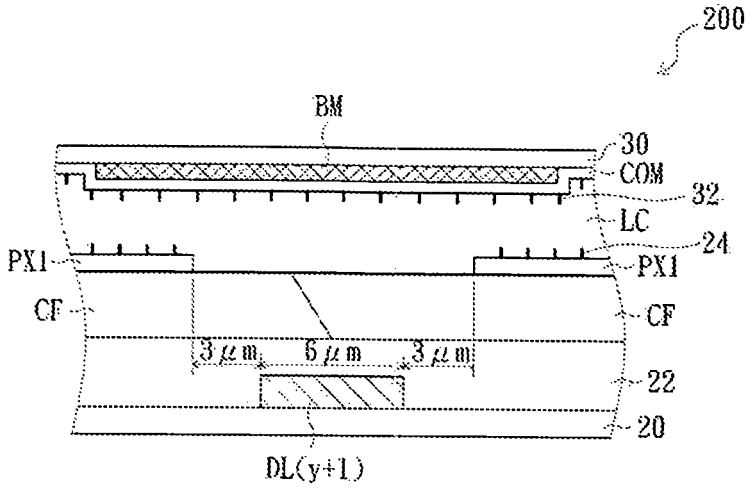

200
BM
30
COM
32
LC
24
PX1
PX1
CF
CF
3 μm
6 μm
3 μm
22
20
DL(y+1)

FIG. 2A

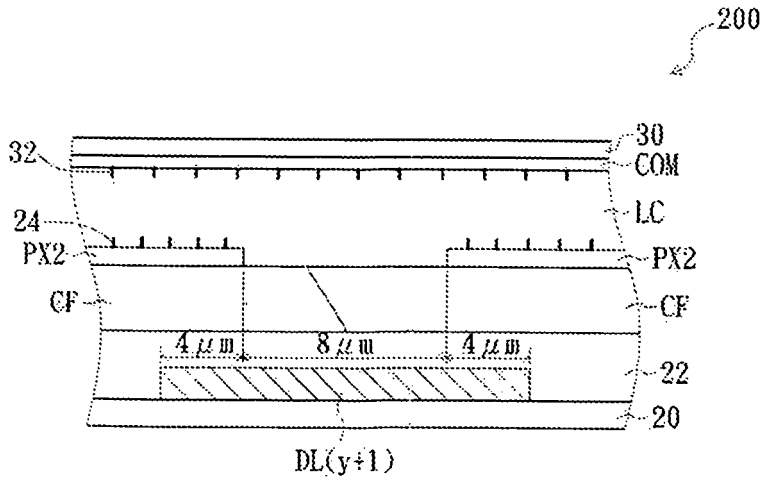

200
32
30
COM
LC
24
PX2
PX2
CF
CF
4 μm
8 μm
4 μm
22
20
DL(y+1)

FIG. 2B

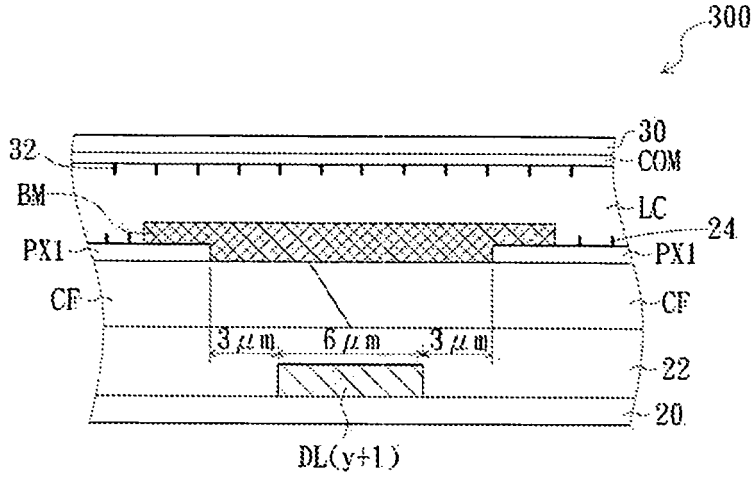

300
32
30
COM
BM
LC
24
PX1
PX1
CF
CF
3㎛
6㎛
3㎛
22
20
DL(y+1)

FIG. 3A

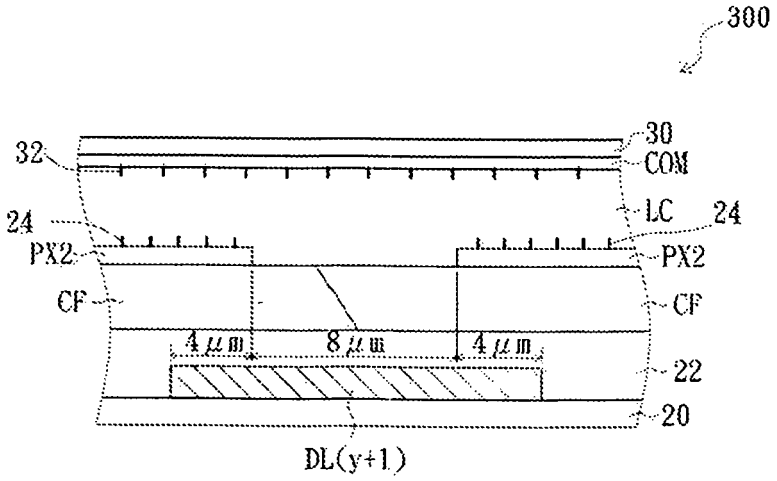

300
32
30
COM
LC
24
24
PX2
PX2
CF
CF
4㎛
8㎛
4㎛
22
20
DL(y+1)

FIG. 3B

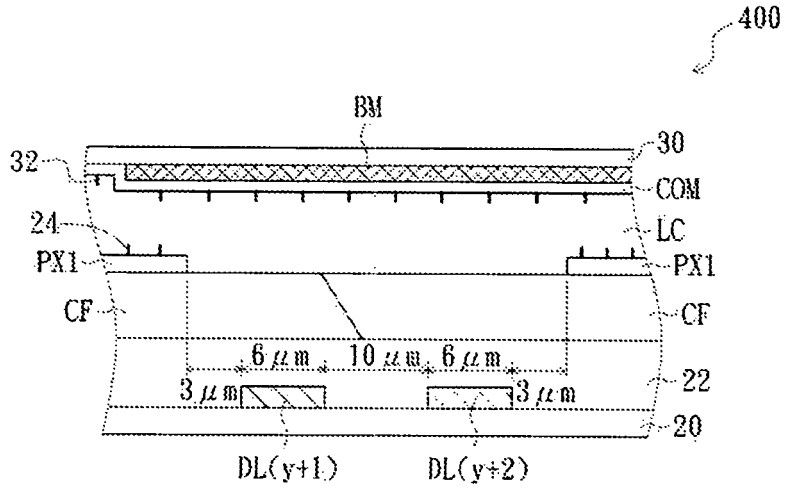

400
BM
30
32
COM
24
LC
PX1
PX1
CF
CF
6 μm
10 μm
6 μm
22
3 μm
3 μm
20
DL(y+1)
DL(y+2)

FIG. 4A

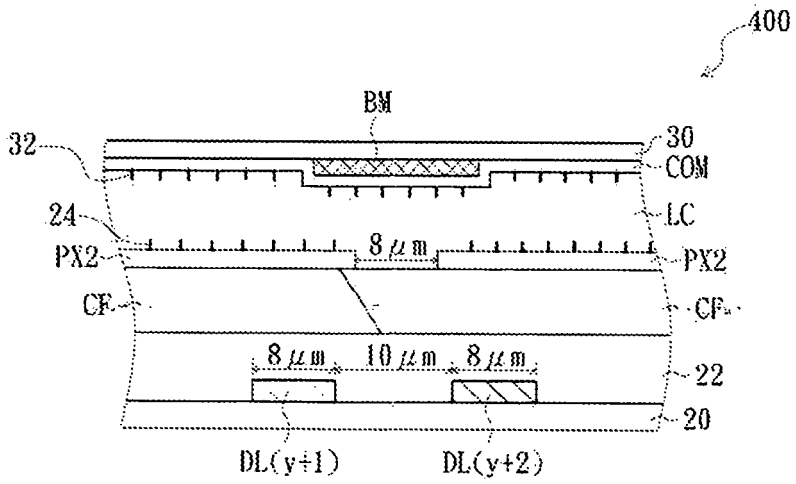

400
BM
32
30
COM
24
LC
8 μm
PX2
PX2
CF
CF
8 μm
10 μm
8 μm
22
20
DL(y+1)
DL(y+2)

FIG. 4B

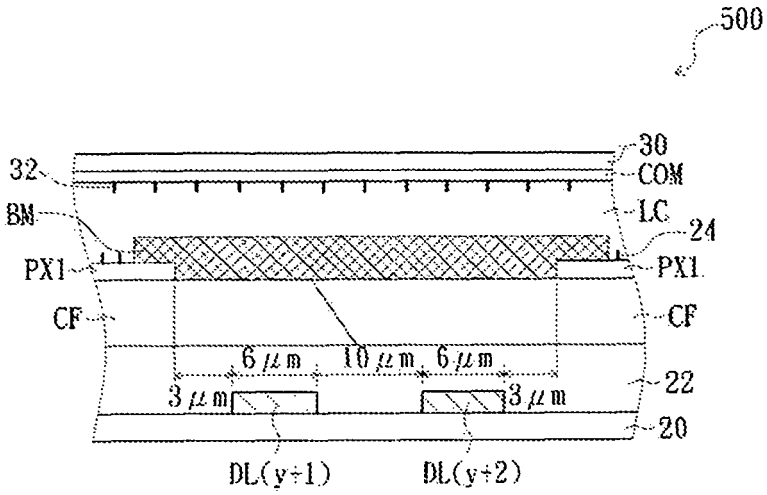

500
32
30
COM
BM
LC
24
PX1
PX1
CF
CF
6 μm
10 μm
6 μm
22
3 μm
3 μm
20
DL(y+1)
DL(y+2)

FIG. 5A

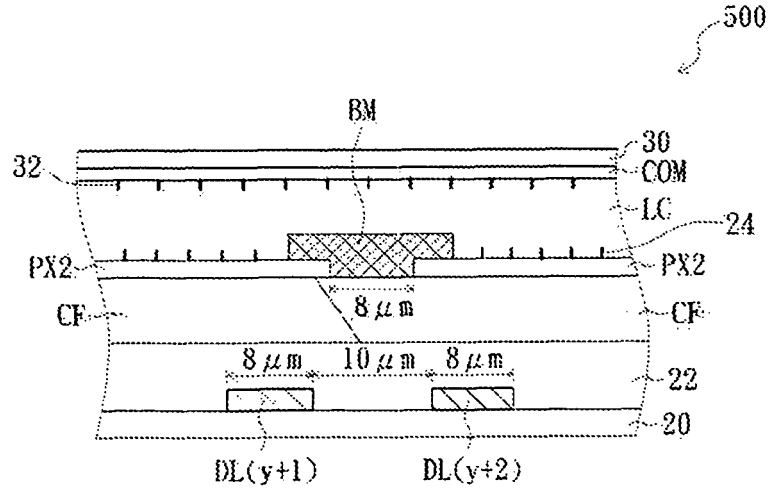

500
BM
32
30
COM
LC
24
PX2
PX2
CF
8 μm
CF
8 μm
10 μm
8 μm
22
20
DL(y+1)
DL(y+2)

FIG. 5B

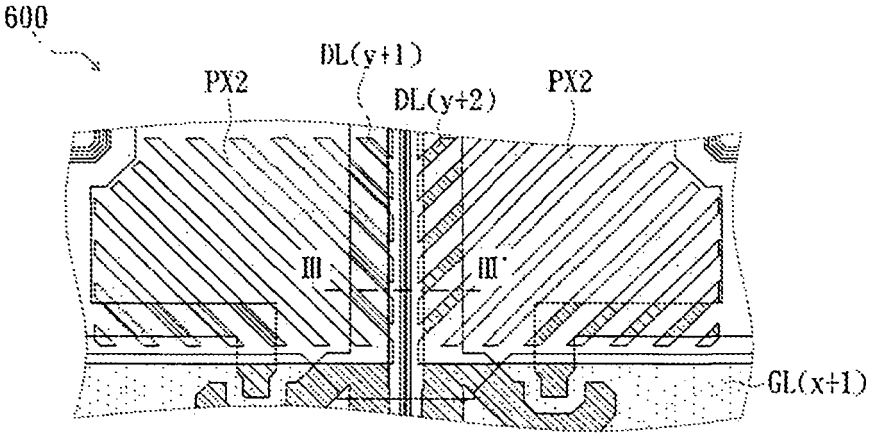

600
DL(y+1)
PX2
DL(y+2)
PX2
III
III'
GL(x+1)

FIG. 6

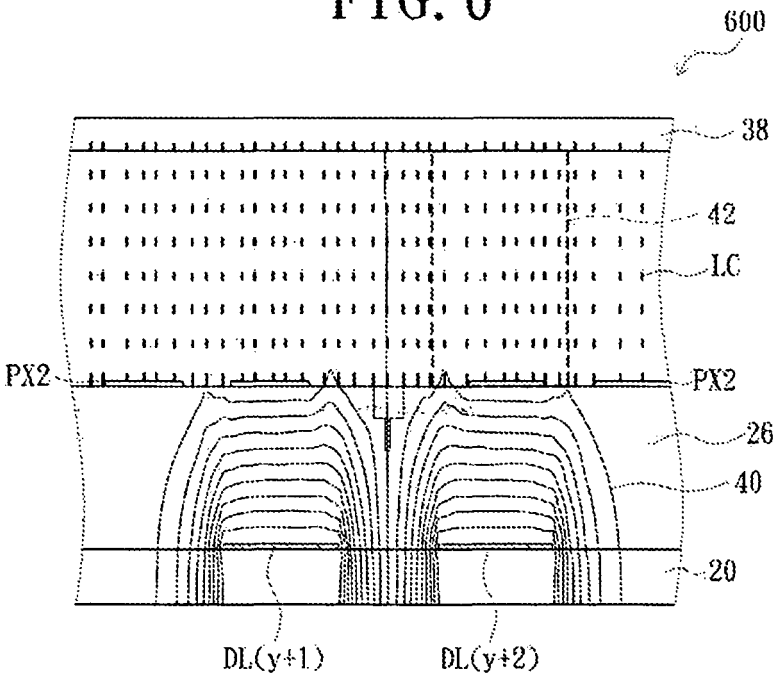

600
38
42
LC
PX2
PX2
26
40
20
DL(y+1)
DL(y+2)

FIG. 7

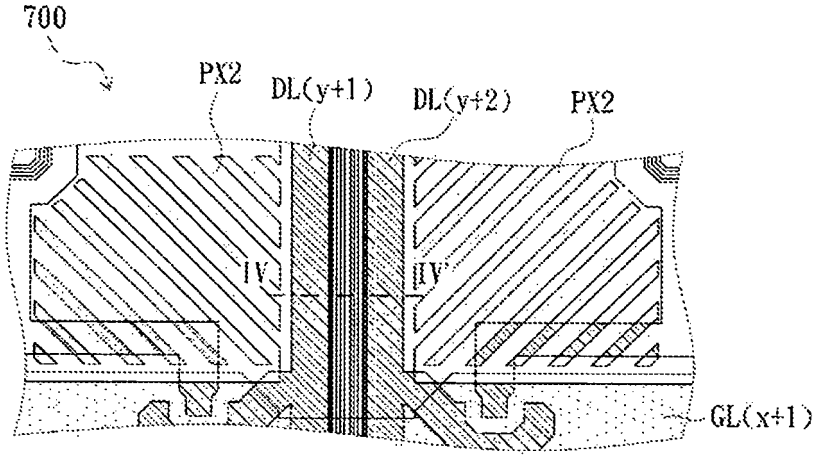

700
PX2
DL(y+1)
DL(y+2)
PX2
IV
IV'
GL(x+1)

FIG. 8

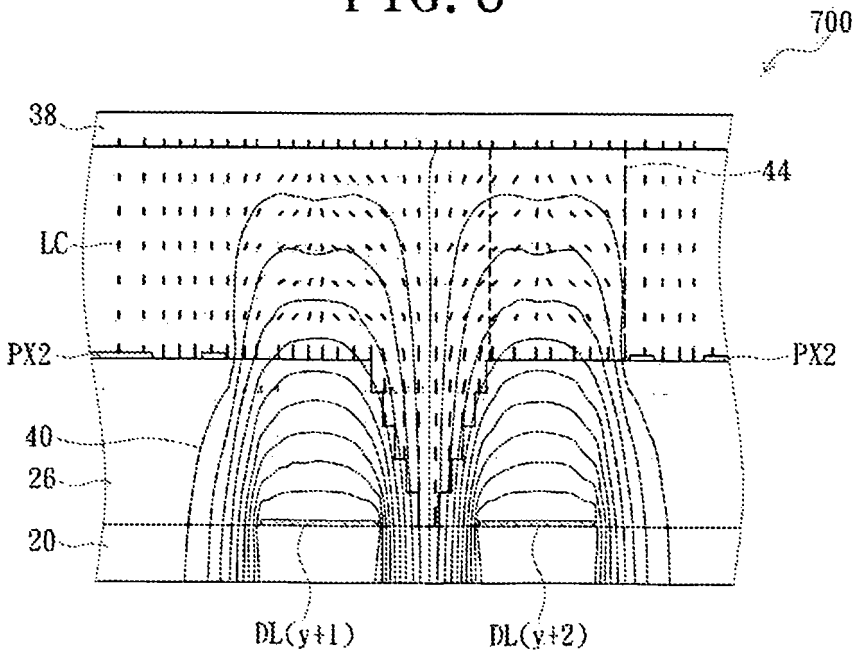

700
38
44
LC
PX2
PX2
40
26
20
DL(y+1)
DL(y+2)

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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